AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A semiconductor device comprising memory cells each having an MISFET for memory selection formed on ~~one~~a major surface of a semiconductor substrate and a capacitive element comprised of a lower electrode electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a first metal layer and an upper electrode formed on said lower electrode via a capacitive insulating film,

wherein said lower electrode has a bottom portion having a thickness greater than a side wall portion of said lower electrode.~~a thickness of 30 nm or greater at the bottom portion thereof.~~

2. (currently amended): A semiconductor device comprising memory cells each having an MISFET for memory selection formed on ~~one~~a major surface of a semiconductor substrate and a capacitive element comprised of a lower electrode electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a first metal layer and an upper electrode formed on said lower electrode via a capacitive insulating film,

wherein said lower electrode has a cup shape ~~of cups~~ provided along a side walls portion and a bottoms portion of a holes provided in an interlayer insulating film and has a bottom

portion having a thickness greater than a side wall portion of said lower electrode~~thickness of 30 nm or greater at the bottom portion thereof~~.

3. (currently amended): A semiconductor device comprising memory cells each having an MISFET for memory selection formed on ~~one~~a major surface of a semiconductor substrate and a capacitive element comprised of a lower electrode electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a first metal layer and an upper electrode formed on said lower electrode via a capacitive insulating film,

wherein said lower electrode has a cup shape ~~of cups~~ provided along a side walls portion and a bottoms~~portion~~ of a holes provided in an interlayer insulating film and has a thickness of 30 nm or greater at the bottom portion of said lower electrode ~~thereof~~ and a thickness of ~~at least~~less than 30 nm ~~or less~~ at a side wall portion of said lower electrode~~thereof~~.

4. (withdrawn/currently amended): A semiconductor device comprising memory cells each having an MISFET for memory selection formed on ~~one~~a major surface of a semiconductor substrate and a capacitive element comprised of a lower electrode electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a first metal layer and an upper electrode formed on said lower electrode via a capacitive insulating film,

wherein said lower electrode has a columnar shape having a cavity in a center portion thereof, and a minimum distance between said cavity and said first metal layer is 30 nm or greater.

5. (withdrawn): The semiconductor device according to any one of claims 1 to 4, wherein said lower electrode has a thickness of 30 nm or greater at least at that portion which contacts said first metal layer.

6. (withdrawn): The semiconductor device according to any one of claims 1 to 4, wherein at that portion of said lower electrode which contacts said first metal layer, there are at most three grain boundaries penetrating said lower electrode in a direction of thickness.

7. (withdrawn): The semiconductor device according to any one of claims 1 to 4, wherein a crystal of said lower electrode at that portion of said lower electrode which contacts said first metal layer has at least 70% of a (002) orientation.

8. (currently amended): A semiconductor device comprising memory cells each having an MISFET for memory selection formed on ~~one~~a major surface of a semiconductor substrate and a capacitive element comprised of a lower electrode electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a first metal layer

and a second metal layer and an upper electrode formed on said lower electrode via a capacitive insulating film,

wherein said lower electrode has a cup shape ~~of cups~~ provided along a side walls portion and a bottomsportion of a holes provided in an interlayer insulating film, said first metal layer and said second metal layer partly contact each other, said lower electrode is connected at only an entire bottom of said lower electrode~~thereof~~ to said second metal layer and said lower electrode has a thickness of 30 nm or greater at the bottom portion of said lower electrode~~thereof~~.

9. (currently amended): A semiconductor device comprising memory cells each having an MISFET for memory selection formed on ~~one~~a major surface of a semiconductor substrate and a capacitive element comprised of a lower electrode electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a first metal layer and a second metal layer and an upper electrode formed on said lower electrode via a capacitive insulating film,

wherein said lower electrode has a cup shape ~~of cups~~ provided along a side walls portion and a bottoms portion of a holes provided in an interlayer insulating film, said first metal layer and said second metal layer partly contact each other, said lower electrode is connected at an entire bottom of said lower electrode~~thereof~~ to said second metal layer and said lower electrode has a thickness of 30 nm or greater at the bottom portion of said lower electrode~~thereof~~ and a thickness of ~~at least~~ less than 30 nm ~~or less~~ at a side wall portion of said lower electrode~~thereof~~.

10. (withdrawn/currently amended): A semiconductor device comprising memory cells each having an MISFET for memory selection formed on ~~one~~a major surface of a semiconductor substrate and a capacitive element comprised of a lower electrode electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a first metal layer and a second metal layer and an upper electrode formed on said lower electrode via a capacitive insulating film,

wherein said first metal layer and said second metal layer partly contact each other, said lower electrode is connected at an entire bottom said lower electrode~~thereof~~ to said second metal layer, said lower electrode has a columnar shape having a cavity in a center portion of said lower electrode~~thereof~~ and a minimum distance between said cavity and said second metal layer is 30 nm or greater.

11. (withdrawn): The semiconductor device according to any one of claims 8 to 10, wherein said lower electrode has a thickness of 30 nm or greater at least at that portion which contacts said second metal layer.

12. (withdrawn): The semiconductor device according to any one of claims 8 to 10, wherein at that portion of said lower electrode which contacts said second metal layer, there are at most three grain boundaries penetrating said lower electrode in a direction of thickness.

13. (withdrawn): The semiconductor device according to any one of claims 8 to 10, wherein a crystal of said lower electrode at that portion of said lower electrode which contacts said second metal layer has at least 70% of a (002) orientation.

14. (withdrawn): The semiconductor device according to any one of claims 8 to 10, wherein said second metal layer is a titanium nitride film.

15. (original): The semiconductor device according to any one of claims 1 through 4 and claims 8 through 10, wherein said lower electrode is a metal film.

16. (original): The semiconductor device according to any one of claims 1 through 4 and claims 8 through 10, wherein said lower electrode is a ruthenium film.

17. (withdrawn): The semiconductor device according to any one of claims 1 through 4 and claims 8 through 10, wherein said lower electrode is a titanium nitride film.

18. (currently amended): The semiconductor device according to any one of claims 1 through 4 and claims 8 through 10, wherein said capacitive insulating film is a ~~titanium nitride~~tantalum oxide film.

19. (original): The semiconductor device according to any one of claims 1 through 4 and claims 8 through 10, wherein said upper electrode is a ruthenium film.

20. (original): The semiconductor device according to any one of claims 1 through 4 and claims 8 through 10, wherein said first metal layer is a titanium nitride film.

21. (withdrawn): The semiconductor device according to any one of claims 1 through 4 and claims 8 through 10, wherein said first metal layer is a tungsten film.

22-48 (cancelled)

49. (new): A semiconductor MIM capacitor comprising:

a lower electrode electrically connected to a metal layer at a bottom portion of said lower electrode, said lower electrode formed on a bottom and side wall surface of a hole in a semiconductor substrate;

a capacitive insulating film formed on said lower electrode; and

an upper electrode formed on said capacitive insulating film,

wherein said bottom portion of said lower electrode has a thickness greater than a side wall portion of said lower electrode.

50 (new): The semiconductor MIM capacitor according to claim 49, wherein said lower electrode has a cup shape.

51. (new): The semiconductor MIM capacitor according to claim 49, wherein said lower electrode has thickness of 30 nm or greater at said bottom portion and a thickness of less than 30 nm at said side wall portion.

52. (new): The semiconductor MIM capacitor according to claim 49; wherein the entire portion of said bottom portion of said lower electrode is connected to said metal layer